**Amendment to the Specification:**

Please amend paragraph [0006] as follows:

[0006] It is preferable that the select circuit incorporates four ~~input terminals~~ inputs, out of which the input ~~terminal~~ for one control signal is linked to an input of a multiplexer, while each of the remaining three ~~input terminals~~ inputs for the other control signals is linked to the input of one of three inverters, while the outputs of the inverters are linked to NAND elements, the outputs of which NAND elements are linked to the other input of the multiplexer and the inputs of another multiplexer, both multiplexers controlled by a signal generated by the processor.

Please amend paragraph [0016] as follows:

[0016] In FIG. 2, the select circuit 4 is disclosed in more detail. The select circuit 4 includes four inputs, namely a first input CE1, a second input BE1, a third input CE2 and a fourth input BE2. The first and second inputs CE1 and BE1 receive data from the processor 3. The third and fourth inputs CE2 and BE2 receive data from the control circuit 2. The first input CE1 is connected to an input of the first multiplexer 26, and to the first inverter 21. The second input BE1 is connected to the first inverter 21. The third input CE2 is connected to an input of the second multiplexer 27. The fourth input BE2 is connected to the third inverter 23. The output of the first inverter 21 is connected to an input of the first NAND element 24, and an input of the second NAND element 25. The output of the second inverter 22 is connected to the other input of the first NAND element 24. The output of the third inverter is connected to the other input of the second NAND element 25. The output of the first NAND element 24 is connected to the other input of the first multiplexer 26. The output of the second NAND element 25 is connected to the other input of the second multiplexer 27. The first and second multiplexers 26, 27 are each controlled by a signal P, from the processor 3.